For immediate release

Tiempo Secure Selects IC'Alps to Accelerate Silicon Implementation of Secure Element IP for IoT Applications

Meylan, FRANCE – April 27, 2021 – Tiempo Secure, a unique supplier of Secure Element IP cores and secure software libraries for semiconductor design companies and IC'Alps, expert in design and supply of application-specific integrated circuits (ASIC), today announced a strategic collaboration to widespread silicon implementation of Common Criteria (CC) EAL5+ grade Secure Element cores for IoT applications. Specifically, Tiempo Secure is relying on IC'Alps' expertise in physical design implementation to develop the hard macro of its Secure Element named TESIC, from netlist to GDSII.

Tiempo Secure's TESIC includes a secure MCU, secure cryptographic processors and hardware accelerators, security sensors, secure memories and standard interfaces for easy integration and test. While TESIC is already available on multiple silicon processes, including GF 55 and TSMC 40, the hard macro is now implemented by IC'Alps in GF 22 and TSMC 16 – with some other technology nodes considered in the coming months.

"By collaborating with IC'Alps for back-end implementation, Tiempo is now able to provide its customers with a wider choice in terms of technology", said Serge Maginot, CEO of Tiempo Secure.

Serge Maginot said IoT applications are driving the demand for a new generation of Secure Elements. Indeed, with billions of IoT devices deployed, it is becoming crucial to secure our connected world with innovative and easy to implement solutions that protect sensitive data from external attacks. Tiempo Secure's TESIC addresses this security concern with a tamper resistant hard macro designed for plug-and-play MCU or SoC integration. TESIC is delivered to the certified fab, with the guarantee chips integrating this macro will pass CC EAL5+ PP0084 and/or EMVCo security certifications.

IC'Alps provides a complete range of semiconductor design services. "We are extremely proud to be partnering with Tiempo Secure", said Jean-Luc Triouleyre, CEO of IC'Alps. "We see a growing trend toward closer ties between IP developers and Design Houses. One reason is that few companies can afford the large investment in EDA software needed for physical implementation tasks." The company offers customers the flexibility to choose an entry point into the ASIC/SoC implementation flow according to their needs, turnaround time, expertise and available EDA environment.

About Tiempo Secure

Tiempo Secure is an independent company headquartered in Montbonnot, near Grenoble, France, with customers in Europe, North America and Asia. It specializes in the development of security intellectual property (IP) in microelectronics and secure embedded software for securing connected devices. The company offers a wide range of Secure Elements IP cores (TESIC family) ready to be integrated into "System-on-Chip" (SoC) components, and allowing maximum security (Common Criteria EAL5+ PP0084 certified) of connected components: authentication on networks with integrated SIM, payment (EMVCo), government or private identification, web authentication (FIDO 2), smart car access, communication with autonomous vehicles (V2X HSM). More information can be found at www.tiempo-secure.com

About IC'Alps

IC'Alps is your one-stop-shop ASIC partner. The company provides customers with a complete offering for Application Specific Integrated Circuits (ASIC) and Systems on Chip (SoC) development from circuit specification, mastering design in-house, up to the management of the entire production supply chain. From its technical centre in France (Grenoble area), IC'Alps supports multiple projects in the demanding medical, industrial, transport, IoT, and mil/aero sectors. The highly qualified engineering teams cover every expertise needed and have a long experience of on-demand analog, mixed-signal and digital integrated circuits on technologies from 0.35 µm down to 16 nm. Moreover, IC'Alps has a proven track record of success with sensor/MEMS AFE interfaces, low power consumption designs, high-resolution converters, signal processing, multiprocessors architectures, hardware accelerators, to name a few. Being a partner of major semiconductor foundries, IP providers, as well as packaging and test houses, IC'Alps is well placed to support customers with full life-cycle solutions. We are proud to be Arm® approved Design Partner, a member of X-FAB's design and supply chain partner network, as well as an Imec IC-link partner. These accreditations assure that we provide expert support and that we have the design expertise to create highly innovative ASIC designs. IC'Alps is ISO 9001, ISO 13485, EN 9100 certified, as well as Common Criteria ready. More information can be found at www.icalps.com